

Application No. Not Yet Assigned

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Docket No. M4065.0019/P019-A

Docket No.: M4065.0019/P019-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Leonard Forbes, et al.

Application No.: Not Yet Assigned

Group Art Unit: 2822

Filed: December 28, 2000

Examiner: M. Trinh

For: HIGH DENSITY SRAM CELL WITH
LATCHED VERTICAL TRANSISTORS



6-23-01
Payton

INFORMATION DISCLOSURE STATEMENT (IDS)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

Pursuant to 37 CFR 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

Those patent(s) or publication(s) listed in the attached form PTO/SB/08 (facsimile) are not supplied because they were previously cited by or submitted to the Office in a prior application no. 09/076,728 filed May 13, 1998 and relied upon in this application for an earlier filing date under 35 U.S.C. 120.

The Commissioner is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0019/P019-A. A duplicate copy of this paper is enclosed.

Dated: December 29, 2000

Respectfully submitted,

By 

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Attorneys for Applicant

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INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)
M4065-0197-29

Application Number
Not Yet Assigned

Applicant(s)
Wendell P. Noble, Jr., et al.

Filing Date
Concurrently Herewith

Group Art Unit
N/A

PTO
12/29/99
12/29/99

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	IF AFTER PRIORITY
		5,173,754	12/1992	M. Manning			
		5,214,295	05/1993	M. Manning			
		5,286,663	02/1994	M. Manning			
		5,486,717	01/1996	Kokubo et al.			
		5,497,011	03/1996	T. Terashima			
		5,535,156	07/1996	Levy et al.			
		5,581,104	12/1996	Lowrey et al.			
		5,594,683	01/1997	Chen et al.			
		5,624,863	04/1997	Helm et al.			
		5,650,350	07/1997	Dennison et al.			
		5,705,843	01/1998	M. C. Roberts			

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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		R. C. Fang, LATCHUP MODEL FOR THE PARASITIC P-N-P-N PATH IN BULK CMOS, IEEE Transactions on Electron Devices, Vol. Ed. 31, No. 1, January 1984,
		R. R. Troutman et al, TRANSIENT ANALYSIS OF LATCHUP IN BULK CMOS, IEEE Transactions on Electron Devices, Vol. Ed. 30, No. 2, February 1993

EXAMINER
Not Yet Assigned

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)

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Group/Art Unit

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,710,741	01/1998	L. McLaury			

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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

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		D. L. Hetherington ET AL, AN INTEGRATED GaAs N-P-N-P THYRISTOR/JFET MEMORY CELL EXHIBITING NONDESTRUCTIVE READ, IEEE Electron Device Letters, Vol. 13, No. 9, September 1992
		S. V. Vandebroek et al, HIGH-GAIN LATERAL BIPOLAR ACTION IN A MOSFET STRUCTURE, IEEE Transactions on Electron Devices, Vol. 38, No. 11, November 1991

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FOREIGN PATENT DOCUMENTS							
	REF	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	Translations YES NO
		No Citations to Foreign Patent Documents					
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
		Dermot MacSweeney et al., MODELING OF LATERAL BIPOLAR DEVICES IN A CMOS,					
		IEEE BCTM 1.4, 4 pages					
		J.J. Ebers, FOUR-TERMINAL P-N-P-N TRANSISTORS, Proceedings of IRE, Nov. 1952, p.1361-4					
		I.T. HO et al, SINGLE THYRISTOR STATIC MEMORY AND ITS FABRICATION, Vol. 23, No.3, 1980					
		B.L. Gregory et al, LATCHUP IN CMOS INTEGRATED CIRCUITS, Sandia Laboratories, p.12-18					
		S. M. Sze, PHYSICS OF SEMICONDUCTOR DEVICES, Second Edition, A Wiley Interscience Pub.					
		S.D. Malaviya, SINGLE-DEVICE DC STABLE MEMORY CELL, IBM Technical Disclosure Bulletin,					
		Vol. 20, No. 9, pp 3492-94, November 1978.					

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